CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A content addressable memory (CAM) cell, comprising:

a matchline;

a wordline; and

a shieldline positioned between said matchline and said wordline for receiving electrical noise from said matchline.

2. The CAM cell of claim 1, wherein said shieldline is coupled to a ground potential.

3. The CAM cell of claim 1, wherein said shieldline is made of metal.

4. The CAM cell of claim 1, wherein said shieldline is made of copper.

5. A content addressable memory (CAM) cell, comprising:

a wordline;

a matchline; and

shielding means for shielding said wordline from noise from said matchline.

6. The CAM cell of claim 5, wherein said shielding means is a conductive material.

7. The CAM cell of claim 6, wherein said shielding means is coupled to a ground potential.

8. A content addressable memory (CAM) cell, comprising:

first and second parallel lines, said first line receiving signals from the CAM cell, said second line providing signals to the CAM cell; and

a conductive structure positioned between the first and second lines and being formed on a same metal layer as the first and second lines, said structure neither receives signals from nor provides signals to the CAM cell and serves to shield said first line from said second line.

9. A content addressable memory (CAM) cell, comprising:

a bitline;

a bitline complement; and

a searchline being positioned substantially symmetrical between said bitline and said bitline complement.

10. The CAM cell of claim 9, wherein said searchline is formed in a first layer in a first plane, and said bitline and said bitline complement are formed in a second layer in a second plane.

11. The CAM cell of claim 10, wherein said first plane is substantially parallel to and above said second plane.

12. The CAM cell of claim 10, wherein said first plane is substantially coplanar to said second plane.

13. A content addressable memory (CAM) cell, comprising:

an input line that receives signals sent to the CAM cell; and

first and second parallel complementary lines that carry complementary signals to and from the CAM cell;

wherein said input line is positioned parallel to and equidistant from said first and second complementary lines.

14. The CAM cell of claim 13 wherein said complementary lines are positioned symmetrically relative to the input line

15. The CAM cell of claim 13 wherein said input line is a searchline.

16. The CAM cell of claim 13 wherein said first and second complementary lines are bitlines.

17. An integrated circuit, comprising:

a content addressable memory (CAM) cell, comprising:

first and second parallel lines, said first line receiving signals from the CAM cell, said second line providing signals to the CAM cell; and

a conductive structure positioned between the first and second lines and being formed on the same metal layer as the first and second lines, said structure neither receives signals from nor provides signals to the CAM cell and serves to shield said first line from said second line.

18. An integrated circuit, comprising:

a content addressable memory (CAM) cell, comprising:

a matchline;

a wordline; and

a shieldline positioned between said matchline and said wordline for receiving electrical noise from said matchline.

19. The circuit of claim 18, wherein said shieldline is coupled to a ground potential.

20. The circuit of claim 18, wherein said shieldline is made of copper.

21. An integrated circuit, comprising:

a content addressable memory (CAM) cell, comprising:

a wordline;

a matchline; and

shielding means for shielding said wordline from noise from said matchline.

22. The circuit of claim 21, wherein said shielding means is a conductive material.

23. The circuit of claim 21, wherein said shielding means is coupled to a ground potential.

24. An integrated circuit, comprising:

a content addressable memory (CAM) cell, comprising:

a bitline;

a bitline complement; and

a searchline being positioned substantially symmetrical between said bitline and said bitline complement.

25. The circuit of claim 24, wherein said searchline is formed in a first layer in a first plane, and said bitline and said bitline complement are formed in a second layer in a second plane.

26. The circuit of claim 25, wherein said first plane is substantially parallel to and above said second plane.

27. The circuit of claim 25, wherein said first plane is substantially coplanar to said second plane.

28. A router, comprising:

a content addressable memory (CAM) cell, comprising:

a wordline;

a matchline; and

shielding means for shielding said wordline from noise from said matchline.

29. The router of claim 28, wherein said shielding means is a conductive material.

30. The router of claim 28, wherein said shielding means is coupled to a ground potential.

31. A router, comprising:

a content addressable memory (CAM) cell, comprising:

a bitline;

a bitline complement; and

a searchline being positioned substantially symmetrical between said bitline and said bitline complement.

32. The router of claim 31, wherein said searchline is formed in a first layer in a first plane, and said bitline and said bitline complement are formed in a second layer in a second plane.

33. The router of claim 32, wherein said first plane is substantially parallel to and above said second plane.

34. The router of claim 32, wherein said first plane is substantially coplanar to said second plane.

35. A processor system, comprising:

a processor; and

a content addressable memory (CAM) cell, comprising:

a wordline;

a matchline; and

shielding means for shielding said wordline from noise from said matchline.

36. The processor of claim 35, wherein said shielding means is a conductive material.

37. The processor of claim 35, wherein said shielding means is coupled to a ground potential.

38. A processor system, comprising:

a processor; and

a bitline;

a bitline complement; and

a searchline being positioned substantially symmetrical between said bitline and said bitline complement.

39. The processor of claim 38, wherein said searchline is formed in a first layer in a first plane, and said bitline and said bitline complement are formed in a second layer in a second plane.

40. The processor of claim 39, wherein said first plane is substantially parallel to and above said second plane.

41. The processor of claim 39, wherein said first plane is substantially coplanar to said second plane.